4.20.3 – 144 Pin, PC133 SDRAM Unbuffered SO–DIMM, Reference Design Specification

PC133 SDRAM Unbuffered SO-DIMM

Reference Design Specification

Revision 1.02

Contents

1. Product Description

This reference specification defines the electrical and mechanical requirements for 144-pin, 3.3 Volt, 133 MHz, 64-bit wide, Unbuffered Synchronous DRAM Small Outline Dual In-Line Memory Modules (SDRAM SO-DIMMs).These SDRAM SO-DIMMs are intended for use as main memory when installed in systems such as mobile personal computers.

Reference design examples are included which provide an initial basis for Unbuffered SO-DIMM designs. Modifications to these reference designs are required to meet all system timing, signal integrity and thermal requirements for 133 MHz support. Other designs are acceptable, and all Unbuffered SO-DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

This specification largely follows the JEDEC defined 144-pin 8-Byte Unbuffered SDRAM SO-DIMM product. (Refer to JEDEC standard 21-C, Section 4.5.6, at www.jedec.org).

Product Family Attributes

SO-DIMM Organization	x 64
SO-DIMM Dimensions (nominal)	67.6 mm (2.66”) x 25.40 mm (1.0”) to x 31.75 mm (1.25”)
Pin Count	144
SDRAMs Supported	64 Mb, 128 Mb, 256 Mb
Capacity	32 MB, 64 MB, 128 MB, 256 MB
Serial PD	Consistent with JEDEC Rev. 2.0
Voltage Options	3.3 volt (V_{DD}/V_{DDQ})
Interface	LVTTL

2. Environmental Requirements

PC133 SDRAM Unbuffered SO-DIMMs are intended for use in mobile computing environments that have limited capacity for heat dissipation.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating Temperature (ambient)	0 to +65	∝C	1
H_{OPR}	Operating Humidity (relative)	10 to 90	%	1
T_{STG}	Storage Temperature	-50 to +100	∝C	1
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	1
	Barometric Pressure (operating & storage)	105 to 69	kPa	1, 2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.

3. Architecture

Pin Description

CK(0:1)	Clock Inputs	2	DQ(0:63)	Data Input/Output	64
CKE(0:1)	Clock Enables	2	DQMB(0:7)	Data Mask	8
RAS	Row Address Strobe	1	V_{DD}	Power (3.3 V)	18
CAS	Column Address Strobe	1	V_{SS}	Ground	18
WE	Write Enable	1	SCL	Serial Presence Detect Clock Input	1
$\overline{S}$(0:1)	Chip Selects	2	SDA	Serial Presence Detect Data Input/Output	1
A(0:9,11:13)	Address Inputs	13	NC	No Connect	8
A10/AP	Address Input/Autoprecharge	1	DU	Don't Use - leave as NC	1
BA0-BA1	SDRAM Bank Address	2		**Total:**	144

Input/Output Functional Description

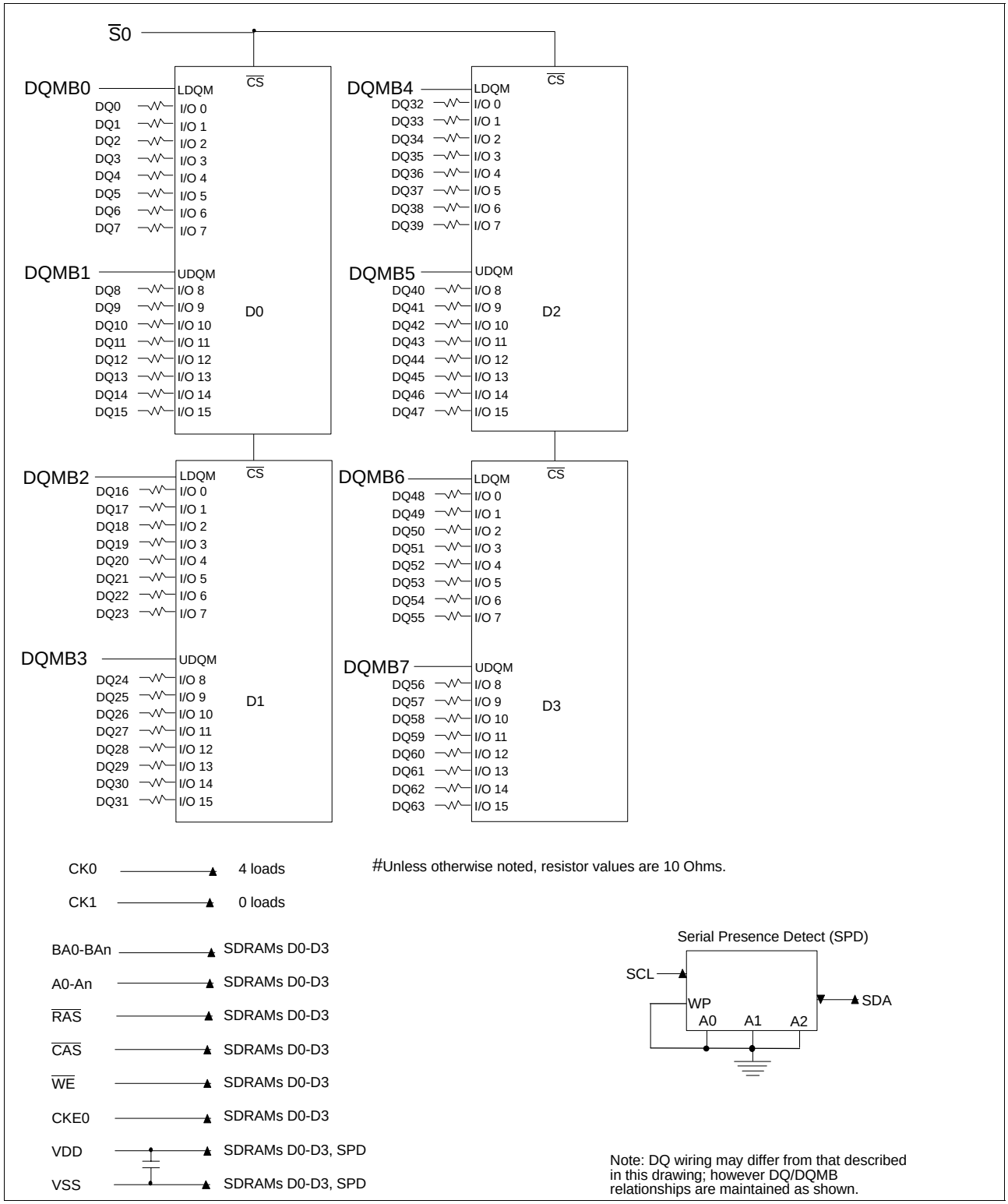
Symbol	Type	Polarity	Function
CK0 - CK1	Input	Positive Edge	The system clock inputs. All of the SDRAM inputs are sampled on the rising edge of their associated clock.
CKE0,1	Input	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, Suspend mode, or the Self Refresh mode.
$\overline{S}0$ - $\overline{S}1$	Input	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Physical Bank 0 is selected by $\overline{S}0$; Bank 1 is selected by $\overline{S}1$.
$\overline{RAS}$, $\overline{CAS}$ $\overline{WE}$	Input	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
BA0, BA1	Input	—	Selects which SDRAM bank of four is activated.
A0 - A9, A11-A13 A10/AP	Input	—	During a Bank Activate command cycle, A0-A13 defines the row address (RA0-RA13) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A11 defines the column address (CA0-CA11) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, then BA0 and BA1 are used to define which bank to precharge.
DQ0 - DQ63	Input Output	—	Data Bit Input/Output pins.
DQMB0 - DQMB7	Input	Active High	The Data Input/Output masks, associated with one data byte, place the DQ buffers in a high impedance state when sampled high. In Read mode, DQMB controls the output buffers like an output enable. In Write mode, DQMB operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high.
V_{DD}, V_{SS}	Supply		Power and ground for the module.
SDA	Input Output	—	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected to V_{DD} to act as a pull up.
SCL	Input	—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from SCL to V_{DD} to act as a pull up.

Unbuffered SDRAM SO-DIMM Pinout

Pin #	Front Side	Pin #	Back Side	Pin#	Front Side	Pin #	Back Side	Pin#	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	V_{SS}	2	V_{SS}	37	DQ8	38	DQ40	73	NU	74	CK1	109	A9	110	BA1
3	DQ0	4	DQ32	39	DQ9	40	DQ41	75	V_{SS}	76	V_{SS}	111	A10/AP	112	A11
5	DQ1	6	DQ33	41	DQ10	42	DQ42	77	NC	78	NC	113	V_{DD}	114	V_{DD}
7	DQ2	8	DQ34	43	DQ11	44	DQ43	79	NC	80	NC	115	DQMB2	116	DQMB6
9	DQ3	10	DQ35	45	V_{DD}	46	V_{DD}	81	V_{DD}	82	V_{DD}	117	DQMB3	118	DQMB7
11	V_{DD}	12	V_{DD}	47	DQ12	48	DQ44	83	DQ16	84	DQ48	119	V_{SS}	120	V_{SS}
13	DQ4	14	DQ36	49	DQ13	50	DQ45	85	DQ17	86	DQ49	121	DQ24	122	DQ56
15	DQ5	16	DQ37	51	DQ14	52	DQ46	87	DQ18	88	DQ50	123	DQ25	124	DQ57
17	DQ6	18	DQ38	53	DQ15	54	DQ47	89	DQ19	90	DQ51	125	DQ26	126	DQ58
19	DQ7	20	DQ39	55	V_{SS}	56	V_{SS}	91	V_{SS}	92	V_{SS}	127	DQ27	128	DQ59
21	V_{SS}	22	V_{SS}	57	NC	58	NC	93	DQ20	94	DQ52	129	V_{DD}	130	V_{DD}
23	DQMB0	24	DQMB4	59	NC	60	NC	95	DQ21	96	DQ53	131	DQ28	132	DQ60
25	DQMB1	26	DQMB5	61	CK0	62	CKE0	97	DQ22	98	DQ54	133	DQ29	134	DQ61
27	V_{DD}	28	V_{DD}	63	V_{DD}	64	V_{DD}	99	DQ23	100	DQ55	135	DQ30	136	DQ62
29	A0	30	A3	65	RAS	66	CAS	101	V_{DD}	102	V_{DD}	137	DQ31	138	DQ63
31	A1	32	A4	67	WE	68	CKE1	103	A6	104	A7	139	V_{SS}	140	V_{SS}
33	A2	34	A5	69	S0	70	A12	105	A8	106	BA0	141	SDA	142	SCL
35	V_{SS}	36	V_{SS}	71	S1	72	A13	107	V_{SS}	108	V_{SS}	143	V_{DD}	144	V_{DD}
Note:															

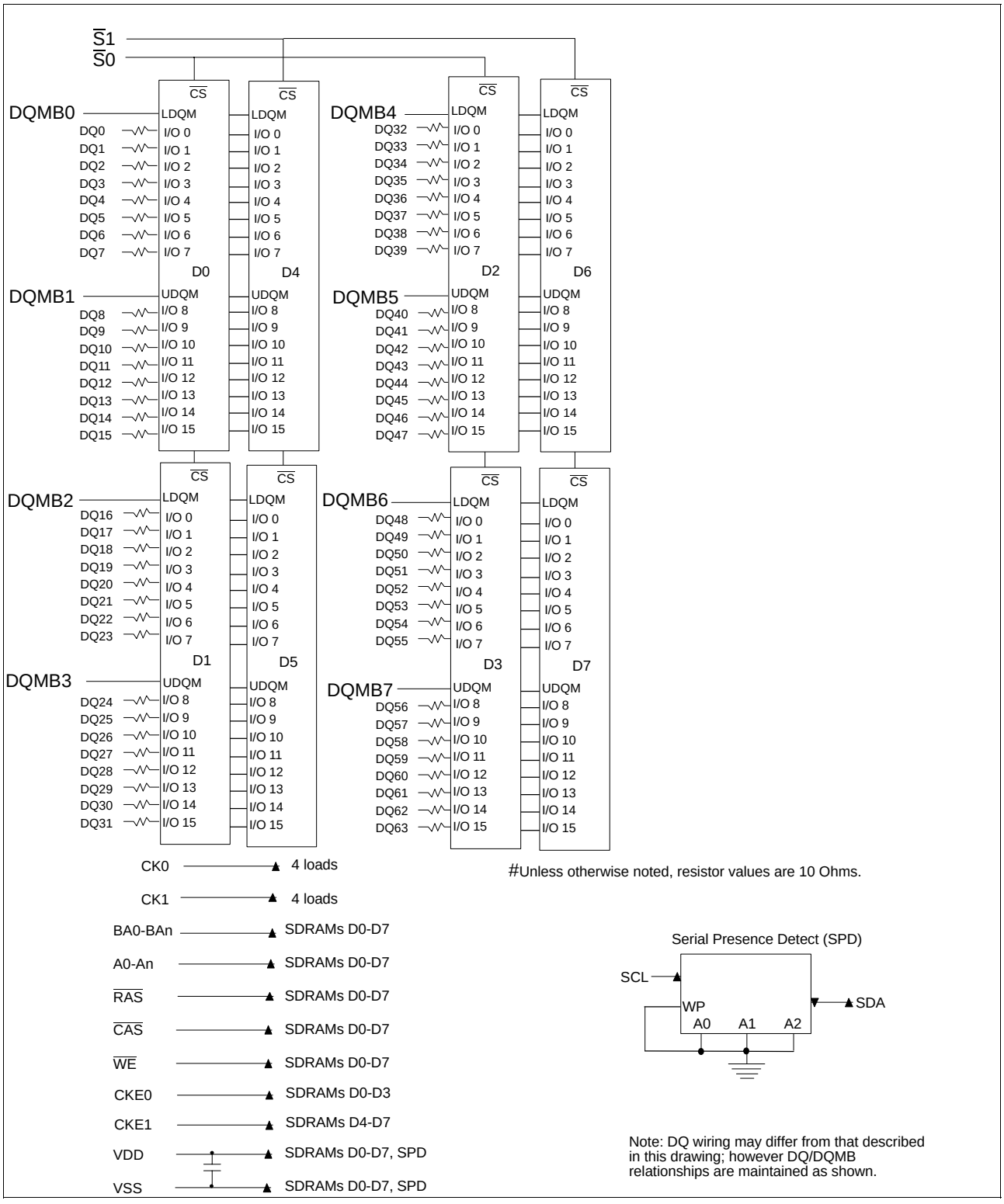
Block Diagram: Raw Card Version A

(Populated as 1 physical bank of x16 SDRAMs)

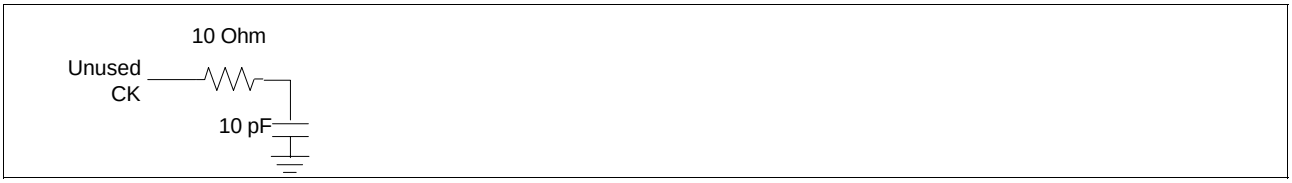


Block Diagram: Raw Card Version B

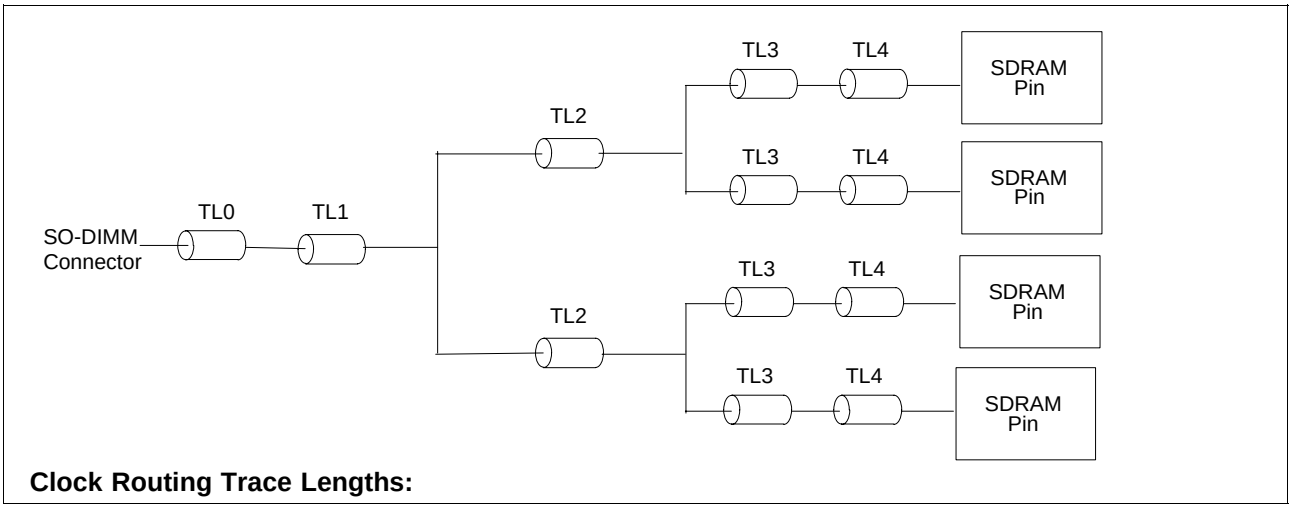
(Populated as 2 physical banks of x16 SDRAMs)



Termination for Unused Clock Signals (0 loads)



Clock Net Wiring (4 loads)

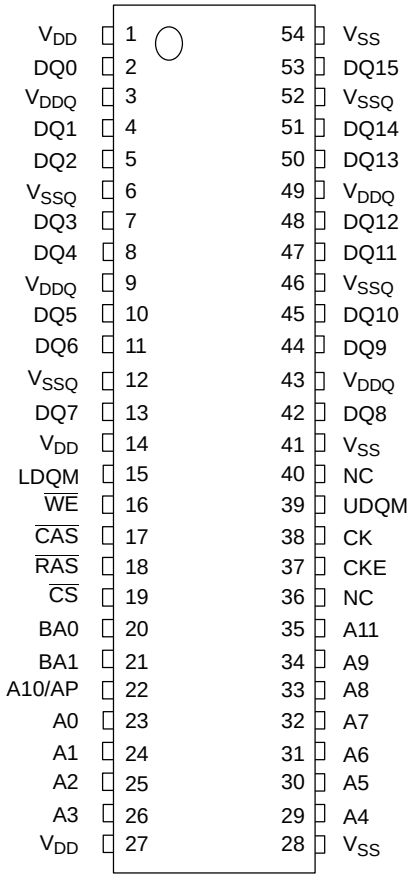


Clock Routing Trace Lengths:

4. Component Details

Pin Assignments for 64 Mb and 128 Mb SDRAM Planar Components

(Top View)



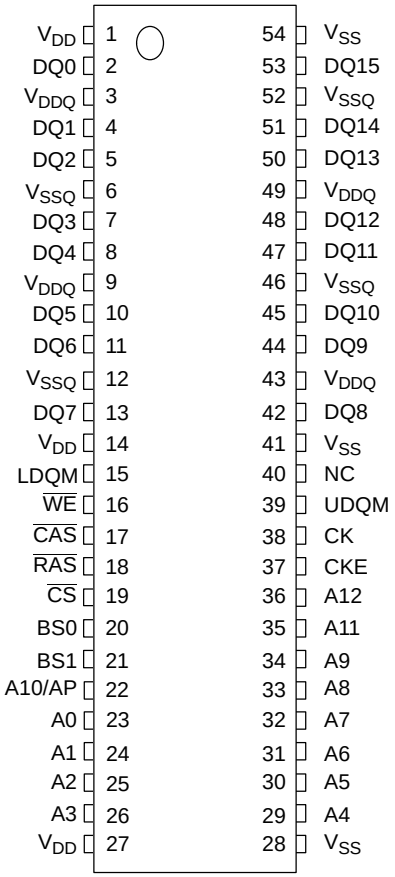
54-pin Plastic
TSOP(II) 400 mil

1 Mb x 16 I/O x 4 Bank
2 Mb x 16 I/O x 4 Bank

Note: Raw Card Versions ‘A’ and ‘B’ support the use of the above SDRAM pin assignments. These pin assignments are consistent with the JEDEC standard package definition.

Pin Assignments for 256 Mb and 512 Mb 54 pin SDRAM Planar Components

(Top View)



54-pin Plastic
TSOP(II) 400mil

4Mb x 16 I/O x 4 Bank

8Mb x 16 I/O x 4 Bank

Note: Raw Card Versions 'A' and 'B' supports the use of the above SDRAM pin assignment. This pin assignment is consistent with the JEDEC standard package.

Reference SDRAM Component Specifications

The 133 MHz SDRAM components used with this SO-DIMM design specification are intended to be consistent with PC133 SDRAM specifications prevalent in the industry. The following is for reference only..

DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	Supply Voltage	3.0	3.6	V	
V_{DDQ}	I/O Supply Voltage	3. 0	3.6	V	
Ii_I	Input Leakage Current ($0 < V_{IN} < V_{DDQ}$)	-10	+1 0	mA	1, 2
I_{CC6}	I_{cc} Low Power (CKE low, all banks closed)	-	2	ma	
V_{OH}	Output High Voltage (I_{OH} = -4 mA)	2.4	-	V	
V_{OL}	Output Low Voltage (I_{OL} = 4 mA)	-	0.4	V	
C_{IN}	Input Pin Capacitance (@1 MHz, 25 °C T_A, 1.4 V bias, 200 mV swing, V_{DD} = 3.3 V)	2.5	3.8	pF	3
$C_{I/O}$	I/O Pin Capacitance(@1 MHz, 25 °C T_A, 1.4 V bias, 200 mV swing, V_{DD} = 3.3 V)	4.0	6.5	pF	4
C_{CK}	Pin Capacitance (@1 MHz, 25 °C T_A, 1.4 V bias, 200 mV swing, V_{DD} = 3.3 V)	2.5	3.5	pF	5
L_{PIN}	Pin Inductance		10	nH	
T_A	Ambient Temperature (No Airflow)	0	65	∞C	

1. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.
2. No Activate or Precharge currents should be included in the Iccac value.
3. Target 3.1 pF
4. Target 4.8 pF
5. Target 3.0 pF

AC Timing Parameters

(T_A = 0-65 ∞C; V_{DD} = 3.0 V - 3.6 V; CL = 2, 3) (Part <$tblsheetnum> of <$tblsheetcount>)

Symbol	Parameter		Speed Grade 100MHz		Speed Grade 133MHz		Units	Notes
			Min	Max	Min	Max		
t_{CK}	Clock Period		10		7.5		ns	
t_{CH}	Clock High Time Rated @1.5V		3		2.5		ns	
t_{CL}	Clock Low Time		3		2.5		ns	
t_{IS}	Input Setup Times	Address/ Command & CKE	2		1.5		ns	
		Data	2		1.5		ns	
t_{IH}	Input Hold Times	Address/Command & CKE	1		0.8		ns	
		Data	1		0.8		ns	
t_{AC}	Output Valid From Clock	$\overline{CAS}$ Latency = 2 or 3, LVTTL levels, Rated @ 50 pF *all outputs switching*		6.0 (tco = 5.2)		5.4 (tco = 4.6)	ns	1
t_{OH}	Output Hold From Clock Rated @ 50 pF (1.8 ns @ 0 pf)		3		2.7		ns	
t_{OHZ}	Output Valid to Z		3	9	2.7	7	ns	
t_{CCD}	CAS to CAS Delay		1		1		t_{CK}	
t_{CBD}	CAS Bank Delay		1		1		t_{CK}	
t_{CKE}	CKE to Clock Disable		1		1		t_{CK}	
t_{RP}	RAS Precharge Time		20		20		ns	
t_{RAS}	RAS Active Time		50		45		ns	
t_{RCD}	Activate to Command Delay (RAS to CAS Delay)		20		20		ns	
t_{RRD}	RAS to RAS Bank Activate Delay		20		15		ns	
t_{RC}	RAS Cycle Time		70		67.5		ns	
t_{DQD}	DQM to Input Data Delay		0		0		t_{CK}	
t_{DWD}	Write Cmd. to Input Data Delay		0		0		t_{CK}	
t_{MRD}	Mode Register set to Active delay		3		3		t_{CK}	
t_{ROH}	Precharge to O/P in High Z			CL		CL	t_{CK}	2
t_{DQZ}	DQM to Data in High Z for read		2		2		t_{CK}	
t_{DQM}	DQM to Data mask for write		0		0		t_{CK}	3
t_{DPL}	Data-in to PRE Command Period		20		15		ns	
t_{DAL}	Data-in to ACT (PRE) Command period (Auto precharge)		5		5		t_{CK}	
t_{SB}	Power Down Mode Entry			1		1	t_{CK}	
t_{SRX}	Self Refresh Exit Time		10		10		ns	4
t_{PDE}	Power Down Exit Set up Time		1		1		t_{CK}	5
t_{CKSTP}	Clock Stop During Self Refresh or Power Down		200		200		t_{CK}	6
t_{REF}	Refresh Period			64		64	ms	7
t_{RFC}	Row Refresh Cycle Time		80.0		75.0		ns	

1. Access times to be measured w/input signals of 1 V/ns edge rate, 0.8 V to 2.0 V, t_{CO} is clock to output with no load.
2. CL = CAS Latency
3. Data Masked on the same clock
4. Self refresh Exit is asynchronous, requiring 10 ns to ensure initiation. Self refresh exit is complete in 10 ns + t_{RC}.
5. Timing is asynchronous. If t_{IS} is not met by rising edge of CK then CKE is assumed latched on next cycle.
6. If the clock is stopped during self refresh or power down, 200 clocks are required before CKE is high.
7. For 64 Mb and 128 Mb SDRAM technology, 4096 refresh cycles. For 256 Mb SDRAM technology, 8192 refresh cycles.

5. Unbuffered SO-DIMM Details

SDRAM Module Configurations (Reference Designs)

Raw Card Version	SO-DIMM Capacity	SO-DIMM Organization	SDRAM Density	SDRAM Organization	# of SDRAMs	SDRAM Package Type	# of Physical Banks	# of Banks in SDRAM	# Address bits row/col/banks
A	32 MB	4MX64	64 Mb	4M X 16	4	54 lead TSOP	1	4	12/8/2
B	64 MB	8Mx64	64 Mb	4M x 16	8	54 lead TSOP	2	4	12/8/2
A	64 MB	8Mx64	128 Mb	8M x 16	4	54 lead TSOP	1	4	12/9/2
B	128 MB	16Mx64	128 Mb	8M x 16	8	54 lead TSOP	2	4	12/9/2
A	128 MB	16Mx64	256 Mb	16M x 16	4	54 lead TSOP	1	4	13/9/2
B	256 MB	32Mx64	256 Mb	16M x 16	8	54 lead TSOP	2	4	13/9/2
A	256 MB	32Mx64	512 Mb	32M x 16	4	54 lead TSOP	1	4	13/10/2
B	512 MB	64Mx64	512 Mb	32M x 16	8	54 lead TSOP	2	4	13/10/2

PC133 Gerber Releases

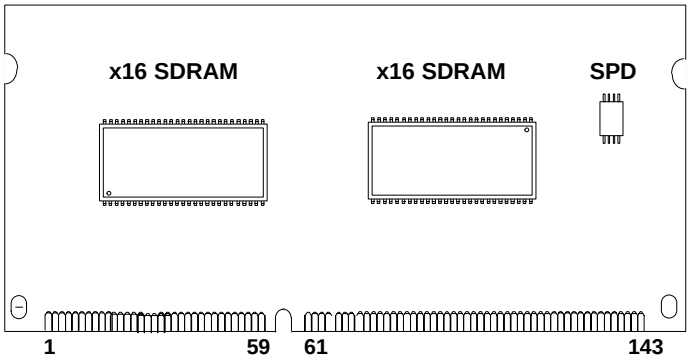
PC133 Unbuffered SO-DIMM gerbers are identical to PC100 Unbuffered SO-DIMM gerbers.

Gerber Revisions

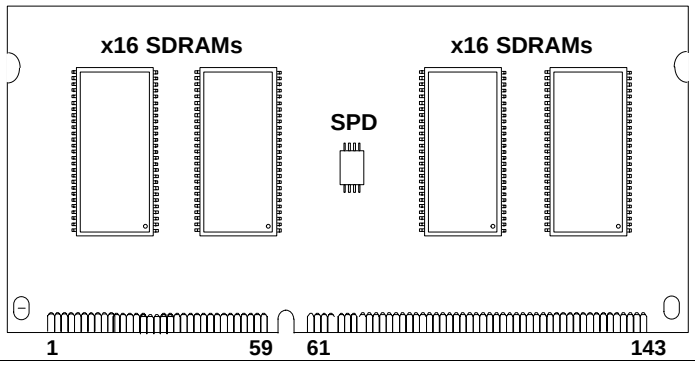
Raw Card	Revision Level	Notes
A	Revision 1.0	
B	Revision 1.0	

Example Raw Card Component Placement

Version A, Front



Version B, Front



6. SO-DIMM Wiring Details

Signal Groups

This reference specification categorizes SDRAM timing-critical signals into seven groups whose members have identical loadings and routings. The following table summarizes the signals contained in each group.

Signal Group	Signals In Group	Page
Clock	CK [1:0]	9
Data	DQ [63:0]	18
Data Mask	DQMB[7:0]	19
Select	$\overline{S}$ [1:0]	20
Clock Enable	CKE [1:0]	21
Address/Control	Ax, BAx, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	22

General Net Structure Routing Guidelines

Net structures and lengths must satisfy signal quality and setup/hold time requirements for the memory interface. Net structure diagrams for each signal group are shown in the following sections. Each diagram is accompanied by a trace length table that lists the minimum and maximum allowable lengths for each trace segment and/or net.

The general routing recommendations are as follows. Other stackups and layouts are possible that meet the electrical characteristics.

- Route all signal traces except clocks using 5/5 rules, i.e., 5 mil traces and 5 mil minimum spacing between adjacent traces.
- Route clocks using at least 90% of the total trace length in the inner layers.
- Route clocks using 5/5 rules with 5 mil ground traces surrounding them. The ground traces are stitched to ground at 0.5” intervals, or as often as routing allows.
- Internal signal layers and the power plane should have a ground ring around the perimeter of the board, stitched to ground at 0.5” intervals. The ground ring should be at least 20 mils wide where layout permits, but can be reduced to 10 mils when necessary.
- No test points are required.

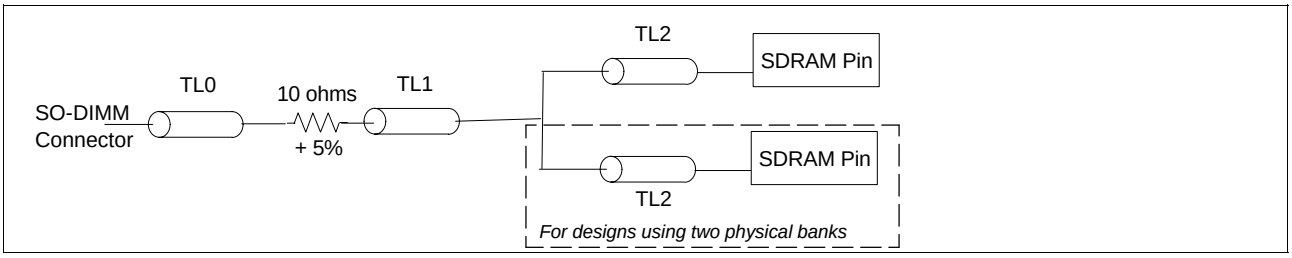
Explanation of Net Structure Diagrams

The net structure routing diagrams provide a reference design example for each raw card version. These designs provide an initial basis for unbuffered SO-DIMM designs. The diagrams should be used to determine individual signal wiring on a SO-DIMM for any supported configuration. Only transmission lines (represented as cylinders and labeled with trace length designators “TL”) represent physical trace segments. All other lines are zero in length. To verify SO-DIMM functionality, a full simulation of all signal integrity and timing is required. The given net structures and trace lengths are not inclusive for all solutions.

Once the net structure has been determined, the permitted trace lengths for the net structure can be read from the table below each net structure routing diagram. Some configurations require the use of multiple net structure routing diagrams to account for varying load quantities on the same signal. All diagrams define one load as one SDRAM input. The net structure routing data in this document accurately represent reference Raw Card versions A and B.

Data Net Structures DQ[63:0]

Net Structure Routing for Data

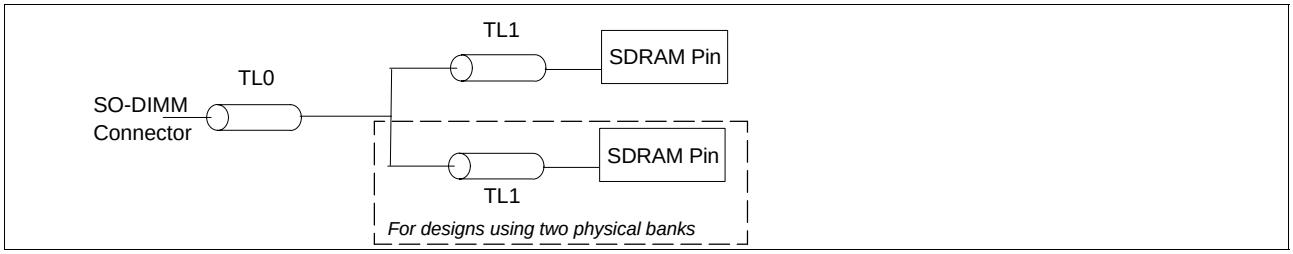


Trace Lengths for Data Net Structure

TL0		TL1		TL2		Total	
Min	Max	Min	Max	Min	Max	Min	Max
0.10	0.50	0	0.90	0	0.25	0.60	1.00
All distances are given in inches and should be kept within a tolerance of ± 0.01 inch							

Data Mask Net Structures, DQMB[7:0]

Net Structure Routing for Data Mask

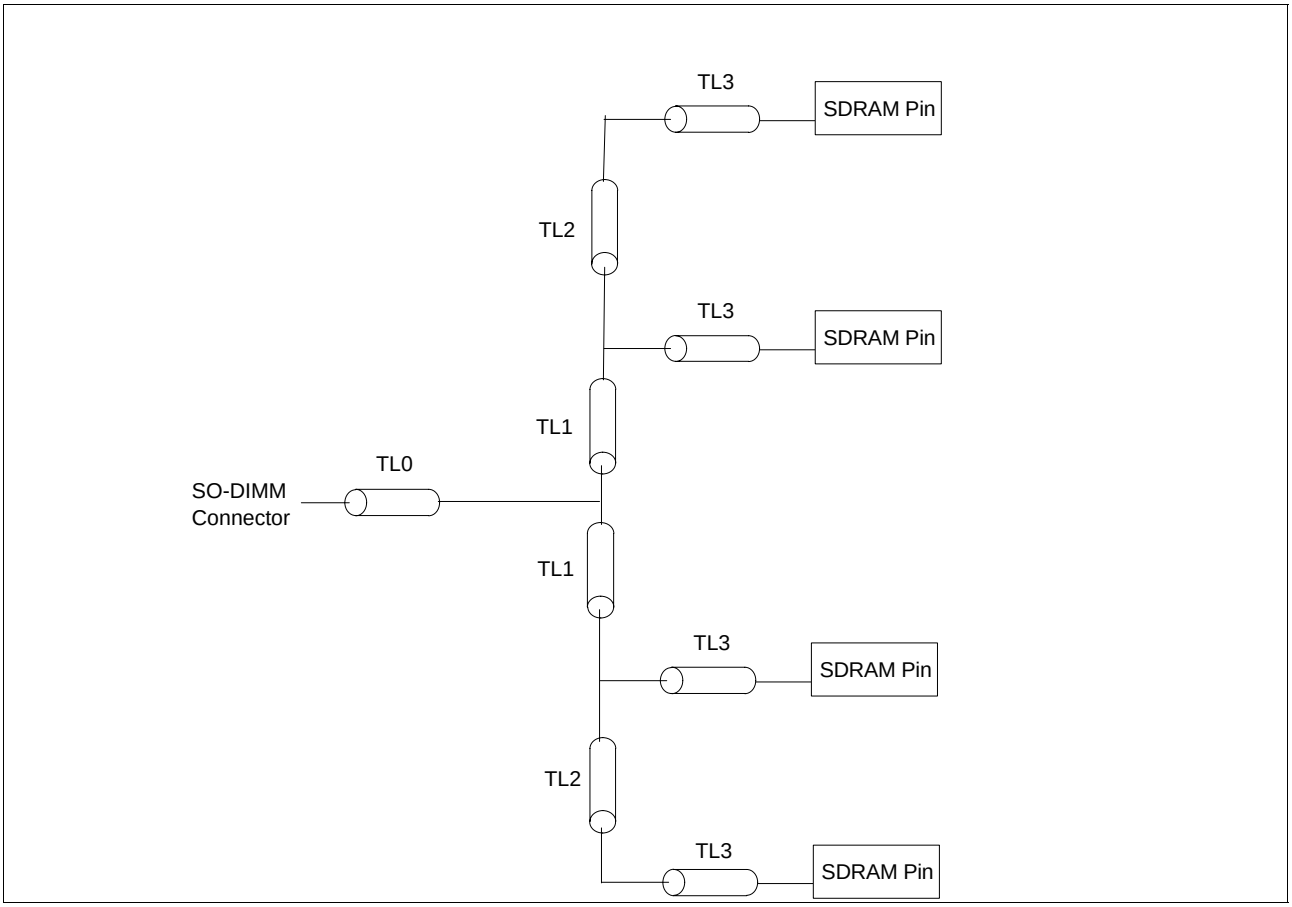


Trace Lengths for Data Mask Net Structures

TL0		TL1		Total	
Min	Max	Min	Max	Min	Max
0.75	1.10	0	0.30	1.00	1.40
All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.					

Select Net Structures $\overline{CS}$ [1:0]

Net Structure Routing for Select

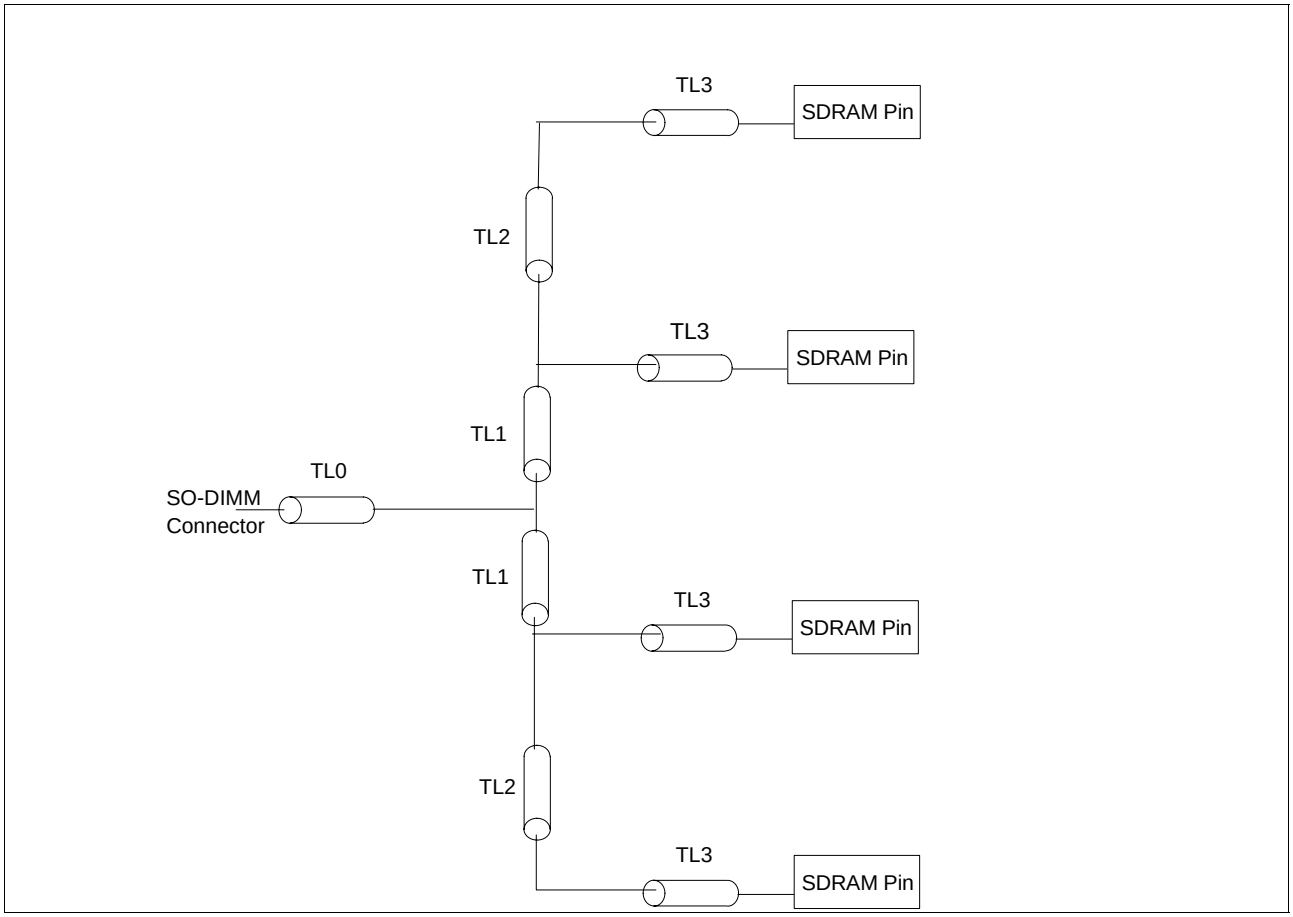


Trace Lengths for Select Net Structures

TL0		TL1		TL2		TL3		Total	
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
0.50	1.10	0.10	0.50	0	0.60	0.05	0.35	1.00	2.30
All distances are given in inches and should be kept within a tolerance of ± 0.01 inches									

Clock Enable Net Structures, CKE [1:0]

Net Structure Routing for Clock Enable



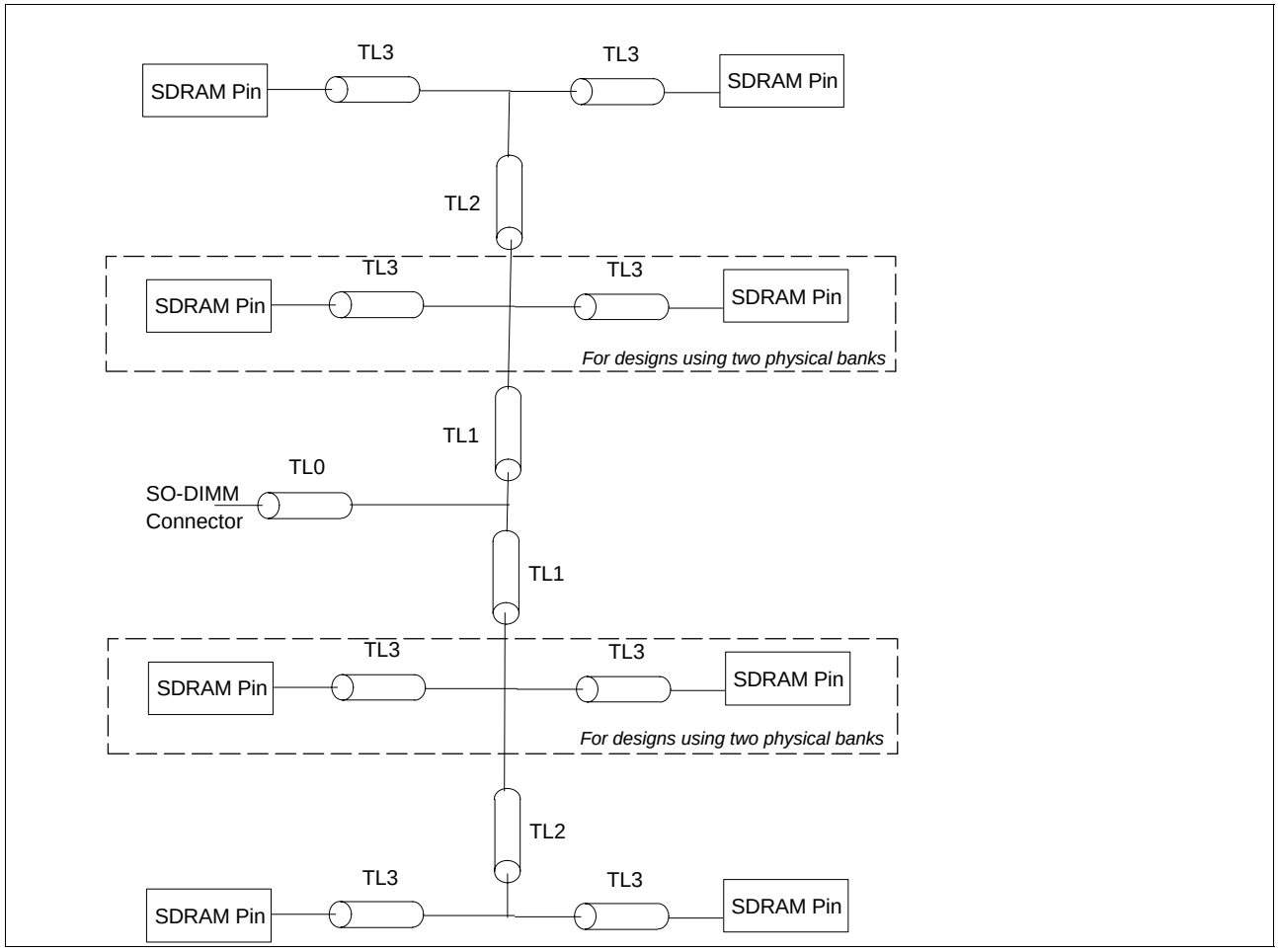
Trace Lengths for Clock Enable Net Structure

TL0		TL1		TL2		TL3		Total	
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
0.50	1.10	0	0.50	0	1.00	0.05	0.35	1.00	2.30

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.

Address/Control Net Structures Ax, BAx, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$

Net Structure Routing for Address and Control



Trace Lengths for Address and Control Net Structures

TL0		TL1		TL2		TL3		Total	
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
0.50	2.50	0	1.10	0	1.00	0.10	0.40	0.75	4.00

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.

Cross Section Recommendations

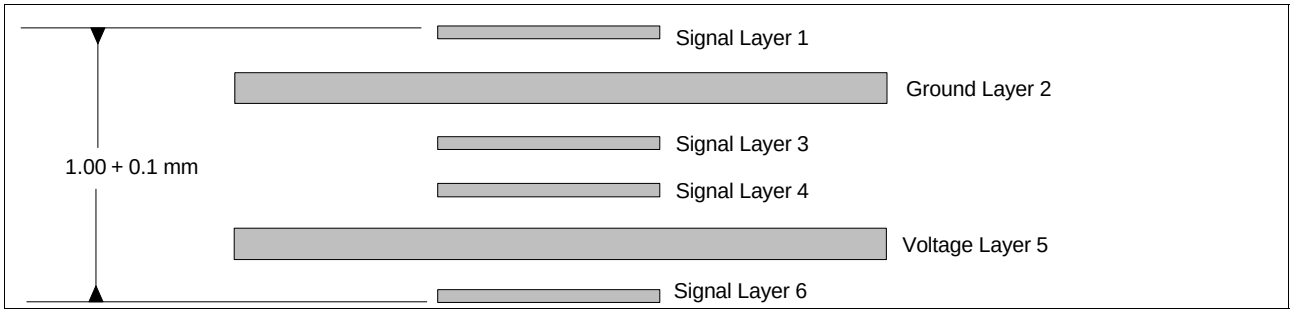
The SO-DIMM printed circuit board design uses six-layers of glass epoxy material. PCBs must contain full ground plane and full power plane layers. The PCB stackup must be designed with 5 mil wide traces. The required board impedance is 55W ± 15%.

Note: The PCB edge connector contacts shall be gold-plated and not chamfered.

PCB Electrical Specifications

Parameter	Min	Max	Units
Trace velocity: S0 (outer layers)	141	153	ps/inch
Trace velocity: S0 (inner layers)	167	180	ps/inch
Trace impedance: Z0 (all layers)	47	63	Ohms

Example Layer Stackup for 5 mil Traces



Component Types and Placement

Components shall be surface mounted on both sides of the PCB and positioned on the PCB to meet the minimum and maximum trace lengths required for SDRAM signals. Bypass capacitors, for SDRAM devices, must be practically located near the device power pins.

7. Serial PD Definition

The Serial Presence Detect function MUST be implemented on the PC SDRAM Unbuffered SO-DIMM. The component used and the data contents must adhere to the most recent version of the JEDEC SDRAM Serial Presence Detect Specifications.

The following table is intended to be an **example** of a typical PC133 SO-DIMM programmed for 3/3/3 (CL/tRP/ tRCD), 133 MHz operation. This SPD table is also programmed with 100 MHz and 66 MHz operation in order to maintain compatibility with these other frequency range operations. SPD values indicating different SO-DIMM performance characteristics, such as CL = 2 operation at 133 MHz, will be utilized based on a specific SO-DIMMs' characteristics.

Serial Presence Detect Data Example

Raw Card Version 'B', 8M x 64 Unbuffered SO-DIMM (Part <$tblsheetnum> of <$tblsheetcount>)

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
0	Number of Serial PD Bytes Written during Production	128	80	
1	Total Number of Bytes in Serial PD device	256	08	
2	Fundamental Memory Type	SDRAM	04	
3	Number of Row Addresses on Assembly	12	0C	
4	Number of Column Addresses on Assembly	9	09	
5	Number of SO-DIMM Banks	1	01	
6 - 7	Data Width of Assembly	x64	4000	
8	Assembly Voltage Interface Levels	LVTTL	01	
9	SDRAM Device Cycle Time (CL = 3)	7.5 ns	75	1
10	SDRAM Device Access Time from Clock at CL= 3	5.4 ns	54	
11	Assembly Error Detection/Correction Scheme	None	00	
12	Assembly Refresh Rate/Type	SR/1X(15.625 μs)	80	
13	SDRAM Device Width	x16	10	
14	Error Checking SDRAM Device Width	Undefined	00	
15	SDRAM Device Attr: Min CK Delay, Random Col Access	1 Clock	01	
16	SDRAM Device Attributes: Burst Lengths Supported	1, 2, 4, 8, Full Page	8F	
17	SDRAM Device Attributes: Number of Device Banks	4	04	
18	SDRAM Device Attributes: $\overline{CAS}$ Latency	2, 3	06	
19	SDRAM Device Attributes: $\overline{CS}$ Latency	0	01	
20	SDRAM Device Attributes: $\overline{WE}$ Latency	0	01	
21	SDRAM Module Attributes	No special	00	
22	SDRAM Device Attributes: General	Write-1/Read Burst, Pre-charge All, Auto-Precharge	0E	
23	Minimum Clock Cycle at CLX-1 (CL = 2)	15.0 ns	F0	1
24	Maximum Data Access Time (t_{AC}) from Clock at CLX-1 (CL = 2)	5.4 ns	54	
25	Minimum Clock Cycle Time at CLX-2 (CL = 1)	N/A	00	
26	Maximum Data Access Time (t_{AC}) from Clock at CLX-2 (CL = 1)	N/A	00	
27	Minimum Row Precharge Time (t_{RP})	20.0 ns	14	
28	Minimum Row Active to Row Active delay (t_{RRD})	15.0 ns	0F	

1. I.Minimum application clock cycle time is 7.5 ns (133 MHz).
2. cc = Checksum Data byte, 00-FF (Hex).
3. ww = Binary coded decimal week code, 01-51 (Decimal) ' 01-34 (Hex).
4. yy = Binary coded decimal year code, 0-00 (Decimal) ' 00-63 (Hex).
5. ss = Serial number data byte, 00-FF (Hex).
6. These values apply to PC100 applications only, per Intel PC66/100 SPD standards.

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
29	Minimum RAS to CAS delay (t_{RCD})	20.0 ns	14	
30	Minimum $\overline{RAS}$ Pulse width (t_{RAS})	45.0 ns	2D	
31	Module Bank Density	128 MB	20	
32	Address and Command Setup Time Before Clock	1.5 ns	15	
33	Address and Command Hold Time After Clock	0.8 ns	08	
34	Data Input Setup Time Before Clock	1.5 ns	15	
35	Data Input Hold Time After Clock	0.8 ns	08	
36 - 40	Reserved	Undefined	00	
41	Minimum Active to Active/Auto Refresh Time (t_{RC})	67 ns	43	
42 - 61	Reserved	Undefined	00	
62	SPD Revision	JEDEC 1.2	12	
63	Checksum for bytes 0 - 62		cc	2
64 - 71	Manufacturers' JEDEC ID Code			
72	Assembly Manufacturing Location			
73 - 90	Assembly Part Number			
91 - 92	Assembly Revision Code			
93 - 94	Assembly Manufacturing Date			3,4
95 - 98	Assembly Serial Number			5
99 - 125	Reserved			
126	Reserved		64	6
127	Reserved		85	6
128 - 255	Open for Customer Use	Undefined	00	

1. I.Minimum application clock cycle time is 7.5 ns (133 MHz).
2. cc = Checksum Data byte, 00-FF (Hex).
3. ww = Binary coded decimal week code, 01-51 (Decimal) ' 01-34 (Hex).
4. yy = Binary coded decimal year code, 0-00 (Decimal) ' 00-63 (Hex).
5. ss = Serial number data byte, 00-FF (Hex).
6. These values apply to PC100 applications only, per Intel PC66/100 SPD standards.

8. Product Label

The following label should be applied to all PC133-compatible SO-DIMMs, to fully describe the key attributes of the module. The label can be in the form of a stick-on label, silk screened onto the assembly, or marked using an alternate customer-readable format. A minimum font size of 8 points should be used, and the number can be printed in one or more rows on the label.

Format:

PC133m-abc-dde-fg

where:

m: Module Type
  S = Unbuffered SO-DIMM (no registers or PLLs on SO-DIMM)
a: SDRAM CAS Latency
b: SDRAM minimum t_{RCD} specification (in clocks)
c: SDRAM minimum t_{RP} specification (in clocks)
dd: SDRAM t_{AC} specification (into 30 pF load), with no decimal point
  54= 5.4 ns t_{AC}
e: JEDEC SPD Revision used on this SO-DIMM
  2 = JEDEC SPD Revision 2.0
f: Gerber file used for this design (if applicable)
  A: Reference design for R/C ‘A’ is used for this assembly
  B: Reference design for R/C ‘B’ is used for this assembly
  Z: None of the ‘Reference’ designs were used on this assembly
g: Revision number of the reference design used:
  1: 1st revision (1st release)
  2: 2nd revision (2nd release)
  3: 3rd revision (3rd release)
  Blank: Not Applicable (used with ‘Z’ above)

Example:

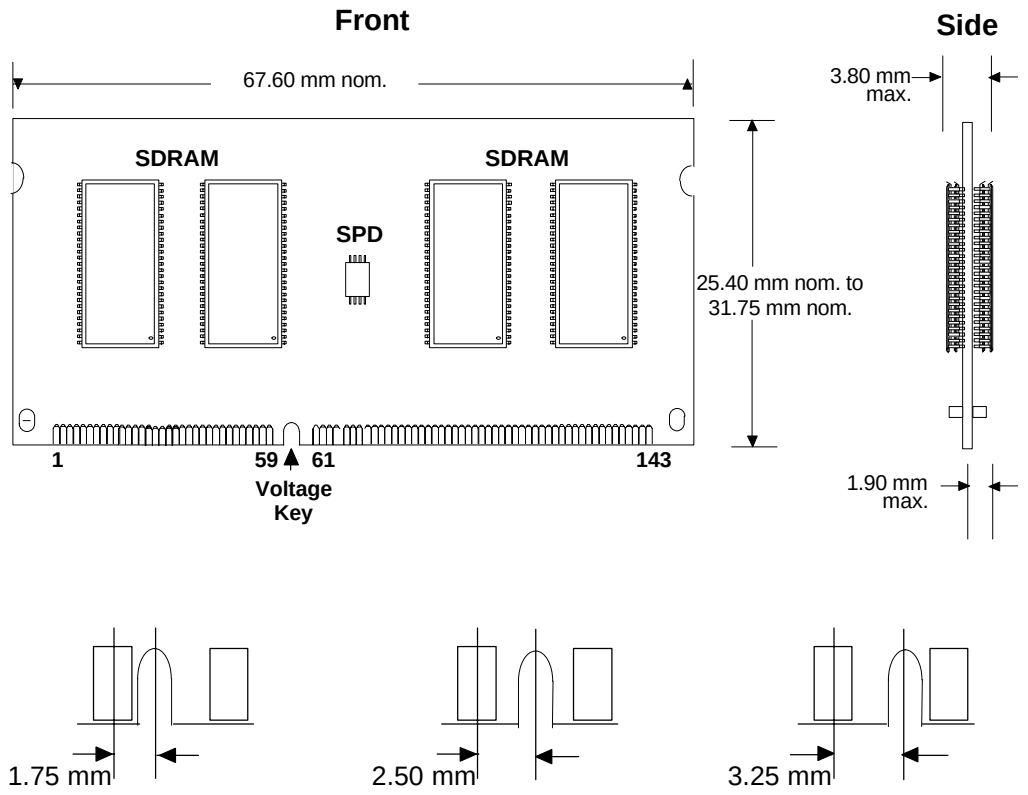
PC133S-333-542-B2
is a PC133 Unbuffered SO-DIMM
with CL = 3, t_{RCD} = 3, t_{RP} = 3
and a t_{AC} = 5.4 ns, using JEDEC SPD Revision 2
and produced based on the ‘B’ raw card Gerber, 2nd release

9. SO-DIMM Mechanical Specifications

JEDEC has standardized detailed mechanical information for the 144 Pin SO-DIMM family. As of the time of this publication, this information can be accessed on the worldwide web as follows:

1. Go to http://www.jedec.org.
2. Click on ‘Free Standards and Docs.’
3. Scroll down and double click on ‘Publication 95.’
4. Under ‘Outlines/Registrations,’ click on ‘Microelectronics Outlines.’
5. Scroll down and select ‘MO-190-C’ to download the PDF for this product family.

Reference Simplified Mechanical Drawing with Keying Position



Note:
The keying defines the SO-DIMM as a 3.3 V Unbuffered SO-DIMM.